Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method in a data processing system for diagnosing errors, said data processing system including a computer which includes a power subsystem and at least one I/O subsystem, said method comprising the steps of:

determining that an error occurred in said at least one I/O subsystem; [[and]]

accessing registers in integrated circuits included within said I/O subsystem utilizing said power subsystem to diagnose said error while said I/O subsystem is in an error state[[.]];

including a power supply controller and at least one power supply in said power subsystem;

said power supply being located in said at least one I/O subsystem; and

including a processor and a JTAG processing engine in said at least one power supply.

2. (Original) The method according to claim 1, wherein said data processing system includes a hardware management computer system coupled to said computer, further comprising:

coupling said hardware management computer system to a central electronics complex that is included within said computer; and

accessing said power subsystem by said hardware management computer system.

3. (Canceled)

4. (Canceled)

5. (Currently amended) The method according to claim 1 [[4]], further comprising:

including within said at least one I/O subsystem an I/O adapter coupled to a first integrated circuit and a second integrated circuit coupled to said first integrated circuit; and

coupling said first and second integrated circuits to said processing engine.

6. (Original) The method according to claim 5, further comprising:

coupling said first and second integrated circuits to said JTAG processing engine utilizing a JTAG/I2C bus.

7. (Original) The method according to claim 1, wherein said data processing system includes a hardware management computer system coupled to said computer, further comprising:

coupling said hardware management computer system to a central electronics complex that is included within said computer;

transmitting a command from said hardware management computer system to said power subsystem to access said at least one I/O subsystem.

8. (Original) The method according to claim 7, further comprising:

receiving said command within a power supply included within said I/O subsystem;

executing said command within said power supply; and

in response to executing said command, accessing, by said power supply, integrated circuits included in said I/O subsystem while said I/O subsystem is in an error state.

9. (Original) The method according to claim 7, further comprising:

including at least one power supply in said power subsystem, said power supply being located in said at least one I/O subsystem;

including a JTAG engine in said at least one power supply;

including within said at least one I/O subsystem an I/O adapter coupled to a first integrated circuit and a second integrated circuit coupled to said first integrated circuit;

coupling said first and second integrated circuits to said JTAG engine utilizing a JTAG/I2C bus;

transmitting said command from said hardware management computer system to said power supply to access said at least one I/O subsystem;

receiving said command within said JTAG engine; and

accessing, by said JTAG engine, either said first or second integrated circuits in response to said JTAG engine processing said command.

10. (Original) The method according to claim 9, further comprising:

reading contents of registers included within either said first or second integrated circuits.

11. (Original) The method according to claim 9, further comprising:

writing data to store in said registers included within either said first or second integrated circuits.

12. (Original) The method according to claim 9, further comprising:

associating a unique JTAG ring number with said first and second integrated circuits; and

determining either said first or second integrated circuits to be accessed utilizing a JTAG ring number associated with said first and second integrated circuits.

13. (Currently amended) A data processing system for diagnosing errors, said data processing system including a computer which includes a power subsystem and at least one I/O subsystem, said system comprising:

said computer including a CPU executing code for determining that an error occurred in said at least one I/O subsystem; [[and]]

said power subsystem for accessing registers in integrated circuits included within said I/O subsystem utilizing said power subsystem to diagnose said error while said I/O subsystem is in an error state[[.]];

a power supply controller and at least one power supply included in said power subsystem;

said power supply being located in said at least one I/O subsystem; and

a processor and a JTAG processing engine included in said at least one power supply.

14. (Original) The system according to claim 13, wherein said data processing system includes a hardware management computer system coupled to said computer, further comprising:

said hardware management computer system coupled to a central electronics complex that is included within said computer; and

said hardware management computer system for accessing said power subsystem.

15. (Canceled)

16. (Canceled)

17. (Currently amended) The system according to claim 13 [[16]], further comprising:

an I/O adapter included within said at least one I/O subsystem, said I/O adapter coupled to a first integrated circuit and a second integrated circuit coupled to said first integrated circuit; and

said first and second integrated circuits coupled to said processing engine.

18. (Original) The system according to claim 17, further comprising:

said first and second integrated circuits coupled to said JTAG processing engine utilizing a JTAG/I2C bus.

19. (Original) The system according to claim 13, wherein said data processing system includes a hardware management computer system coupled to said computer, further comprising:

said hardware management computer system coupled to a central electronics complex that is included within said computer;

said hardware management computer system transmitting a command to said power subsystem to access said at least one I/O subsystem.

20. (Original) The system according to claim 19, further comprising:

said power supply included within said I/O subsystem for receiving said command;

said power supply for executing said command; and

in response to executing said command, said power supply for accessing integrated circuits included in said I/O subsystem while said I/O subsystem is in an error state.

21. (Original) The system according to claim 19, further comprising:

at least one power supply included in said power subsystem, said power supply being located in said at least one I/O subsystem;

a JTAG engine included in said at least one power supply;

an I/O adapter included within said at least one I/O subsystem, said I/O adapter coupled to a first integrated circuit and a second integrated circuit coupled to said first integrated circuit;

said first and second integrated circuits coupled to said JTAG engine utilizing a JTAG/I2C bus;

said hardware management computer system for transmitting said command to said power supply to access said at least one I/O subsystem;

said JTAG engine for receiving said command; and

said JTAG engine for accessing either said first or second integrated circuits in response to said JTAG engine processing said command.

22. (Original) The system according to claim 21, further comprising:

said JTAG engine for reading contents of registers included within either said first or second integrated circuits.

23. (Original) The system according to claim 22, further comprising:

said JTAG engine for writing data to store in said registers included within either said first or second integrated circuits.

24. (Original) The system according to claim 21, further comprising:

a unique JTAG ring number associated with said first and second integrated circuits; and

said JTAG ring number being utilized to determine either said first or second integrated circuits to be accessed.

25. (Currently amended) A computer program product comprising:

a computer-readable storage medium including computer usable program code for diagnosing errors in a data processing system that includes a computer, which includes a power subsystem and at least one I/O subsystem; said computer program product including ~~comprising~~:

~~providing a data processing system that includes a computer which includes a power subsystem and at least one I/O subsystem~~

computer usable program code ~~instruction means~~ for determining that an error occurred in said at least one I/O subsystem; [[and]]

computer usable program code ~~instruction means~~ for accessing registers in integrated circuits included within said I/O subsystem utilizing said power subsystem to diagnose said error while said I/O subsystem is in an error state[[.]];

including a power supply controller and at least one power supply in said power subsystem;

said power supply being located in said at least one I/O subsystem; and

including a processor and a JTAG processing engine in said at least one power supply.